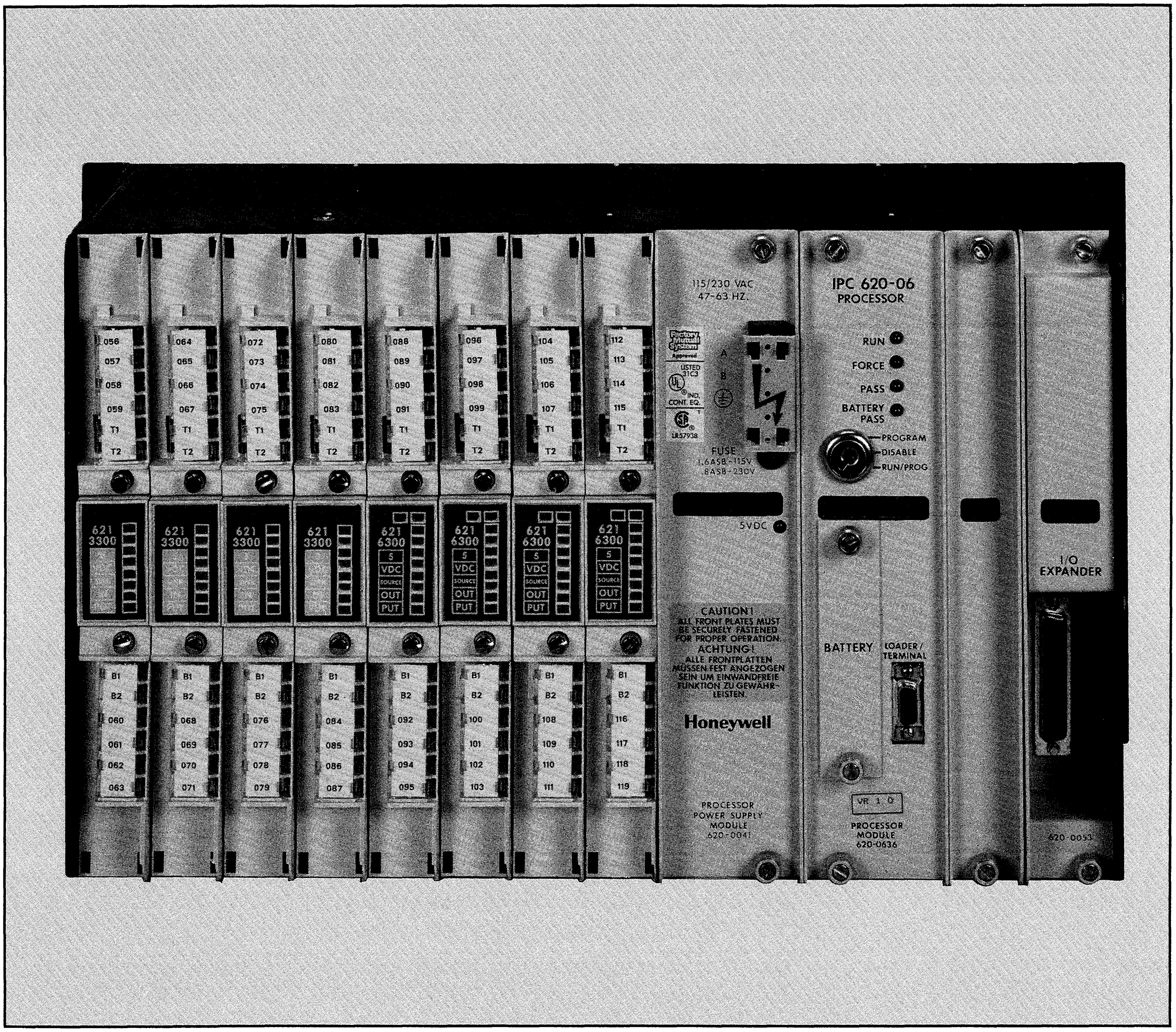
620
Programmable
Controller System

Form No. 620-8975
Rev. A
5/89
Supersedes:
Nothing

IPC 620
Programmable Controller
Model IPC 620-06

User Manual



INDUSTRIAL CONTROLS DIVISION

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USER MANUAL CROSS REFERENCE FOR IPC 620-06 PROCESSORS

MANUAL:	MATERIAL COVERED:
IPC 620 Installation User Manual Form No. 620-8996	620 system overview; system configuration for all processor models, parallel and serial I/O; addressing; rack assembly mounting; module settings (jumpers and DIP switches); module installation; cable and conduit routing; wiring; reference information on superseded model numbers.
IPC 621 I/O Specifications User Manual Form No. 620-8995	I/O system overview; detailed module descriptions (digital input, digital output, special function); serial I/O system; fuse and battery requirements.
IPC 623-6000 Loader/Terminal User Manual Form No. 623-8987	Hardware description; installation; modes of operation; programming instructions and examples; editing and display functions; documentation and tape functions; trouble-shooting and maintenance; codes and error messages.
IPC 623-60 MS-DOS Loader User Manual Form No. 623-8986	Product description and requirements; installation and configuration; system start-up and menus; IPC 620 instruction set; edit and display functions; program editing instructions; documentation; utility functions; applies to loader with version 3.0 of MS-DOS, which is compatible with all 620 PLC's.

INTRODUCTION

The IPC 620 Programmable Controller System fulfills three important factory automation requirements:

- Control
- Communication
- Monitoring

The 620 System consists of seven control processors, a universal I/O system, a programming device (623-6000 Loader/Terminal and 623-60 MS-DOS Loader software), industrial microcomputers plus related software products, and communication systems.

This user manual deals specifically with the 620-06 processor. Other 620 System items -- the 623-6000 Loader/Terminal, the 623 MS-DOS Loader software, IPC 627 LOS User Manual, motion control products, 620 Control Network, and the other 620 processors are supported by their own literature.

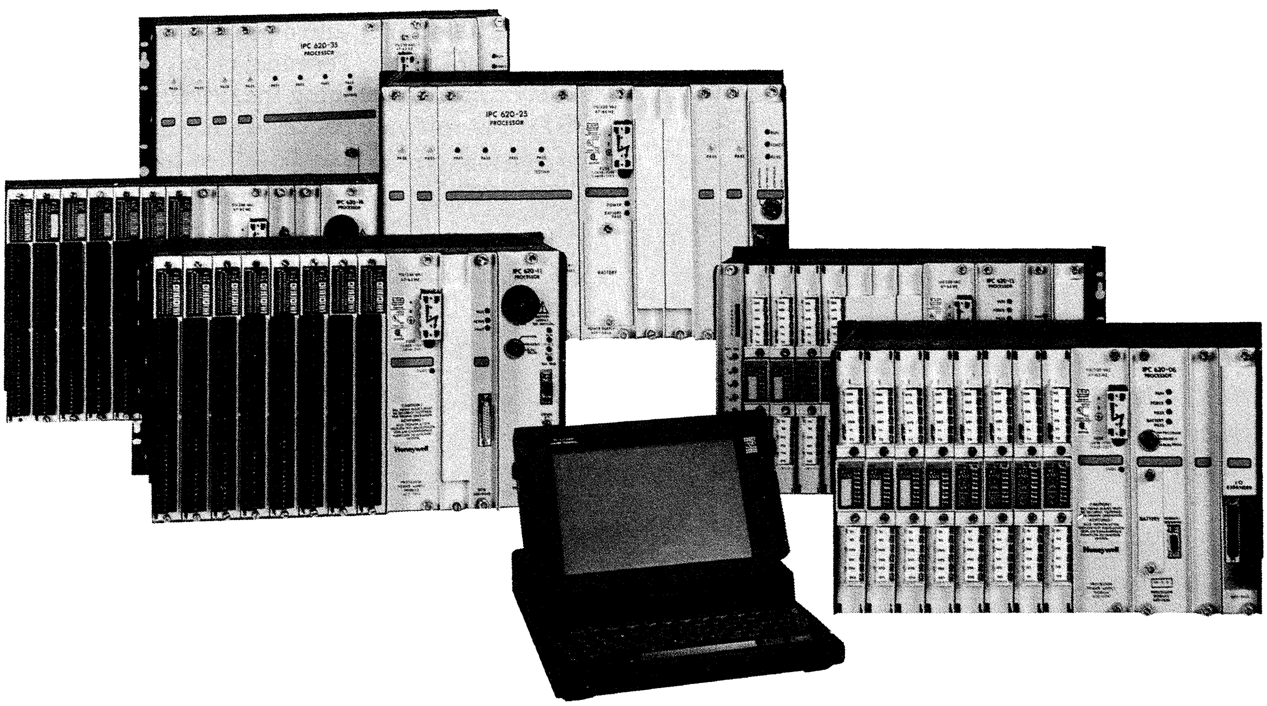


FIGURE 1 - 620 SYSTEM

PROCESSOR RACKS

Model No. 620-0090
620-0091
620-0092
620-0093

These processor racks are rugged steel cardracks that house a 620-06 Processor Module, Power Supply Module, I/O Modules, the I/O Expander Module, and an option module. The card slots are labeled A through N in the full rack and A-H in the half rack. See Figure 2.

The 620-0090 Processor Rack is the standard rack capable of holding up to eight I/O modules. The 620-0091 Augmented Processor Rack can also contain up to eight I/O modules and includes an additional upper local bus on the backplane to facilitate communication between modules equipped for dual bus communication (ie. Servo modules).

The 620-0092 Processor Half Rack is the standard rack capable of holding up to four I/O modules. The 620-0093 Augmented Processor Half Rack can also hold up to four I/O modules. Half racks do not support I/O Expander Modules or option modules, and they use either the 621-9932 or 621-9934 Power Supply Modules.

Each processor full rack fits into an 8-inch deep enclosure, or a 19-inch instrumentation rack. The rack conforms to the "HE" standard. Reversible mounting brackets allow the rack to be rack or panel mounted. When the brackets are attached to the rack front, it mounts in a standard 19-inch rack. When the brackets are rotated 180° and mounted to the rear, the rack can be panel mounted.

All cardrack connectors are offset to prevent installing a module upside down.

OPTION MODULES

Slot M of the processor rack is available for an option module. A Control Network Module, a Communications Interface Module, a Data Collection Module, an Operator Panel Interface Module or a Hiway Interface Module may be used. Empty option slots must be protected with the blank coverplates supplied. <u>The I/O Expander Module is required if an option module is used.</u>

Control Network Module (CNM)

Model No. 620-0038

A CNM may be installed in option slot M. This module allows I/O status to be shared between as many as eight 620 processors over a high speed serial link. Each system with a CNM installed may transmit 32 I/O status bits (or 64 depending on the number of systems in the network) to other processors on the Control Network. Each CNM reserves up to 256 I/O status bits in the Control Relay Table to store I/O status from other processors on the link. See Control Network/Intro User Manual (Form No. 620-8994).

Communications Interface Module (CIM)

Model No. 620-0043 (Form No. 620-8986)
Modubus RTU Protocol
620-0044 (Gateway Manual)
Honeywell DMCS Protocol
620-0048 (Form No. 620-8980)
Honeywell ABC Protocol
620-0052 (Form No. 620-8980)
Honeywell ABC Protocol

The Communications Interface Modules allow serial communication between the 620-06 system and the 627 products or other intelligent devices. The Data Collection Modules (620-0048 and 620-0052) are specialized CIM's that have instructions for collecting data from the PLC Status Table. See the appropriate CIM user manual.

Hiway Interface Module (HIM)

The HIM is an interface between an IPC 620 Processor and Honeywell's TDC-3000 Data Hiway. The HIM provides a service facility for higher order devices in the system, such as computers and operator stations to interface with the IPC 620 Processor. The HIM is supported by the user manual, Form 620-8981.

Operator Panel Interface Module (OPI)

The OPI is an interface module that connects field devices, such as pushbuttons and keypad displays to the processor through a single coaxial cable. The OPI is supported by the user manual, Form 621-0989.

PROCESSOR MODULE (PM)

Model No. 620-0636

The 620-06 Processor Module is a self-contained single module processor consisting of a logic processor, program memory, a 16-bit register area and an I/O status area.

A battery compartment in the PM contains a size AA lithium dry cell battery which provides backup power to the Memory and Register area. This battery is installed when the PM is shipped. The battery is front-accessible by removing the BATTERY coverplate. The output is 3.0 volts and will sustain both the Memory and Register Tables for a minimum of 6 months.

CAUTION

Lithium batteries are prohibited from passenger aircraft. The following conditions are potentially hazardous and should be avoided:

- Recharge
- Incineration
- Short circuit
- Forced overcharge (reversal)
- Use or storage outside of the specified temperature range.
- Puncturing, crushing or disassembling

NOTE

An insulating wafer prevents battery discharge during shipment and storage and must be removed before system operation.

The processor's frontplate contains a 3-position mode control keyswitch with PROGRAM, DISABLE and RUN/PROGRAM. Four status LED's indicate the following information.

- A RUN LED indicates that the 620-06 is scanning.
- The FORCE LED signifies that one or more program instructions are in the forced state.
- The PASS LED indicates passing module self-test.
- The LED labeled BATTERY PASS indicates that the battery is good.

The 9-pin D connector is the Loader/Terminal connection point. This port is configured for RS422 operation and a 9600 Baud data rate. Refer to the 623-6000 LOADER/TERMINAL USER MANUAL (Form 623-8987) or the 623-60 MS-DOS LOADER USER MANUAL Form 623-8986.

The PM consists of two printed circuit boards. The smaller of the two, the processor printed circuit board, contains a Motorola 68B09E microprocessor, program memory, and data tables.

CAUTION

RAM memory rentention is not guaranteed when the Processor Module is removed from the rack. Even if the battery remains installed, stray static voltages may occur, resulting in memory changes. In these cases, a checksum fault is detected.

Memory - 2K

The system's Output Status Data Table contained on the processor printed circuit board accommodates the status of 768 output locations. The output status of real I/O is contained in locations 0-191 and control relay status in locations 192-767. Timer and counter presets and accumulated values plus other data is contained in the Register Table at addresses 4096-4351 which are 16 bits wide. Figure 3 illustrates the memory distribution. Table 1 describes the system capacities of real I/O, control relay addresses and 16-bit registers.

TABLE 1 - SYSTEM I/O AND REGISTER CAPACITIES

SYSTEM MEMORY SIZE	BIT ADDRESSES		16-BIT REGISTERS
	MAXIMUM REAL I/O CAPACITY	NUMBER OF CONTROL RELAY ADDRESSES (in addition to real I/O)	
2K	192	576	256

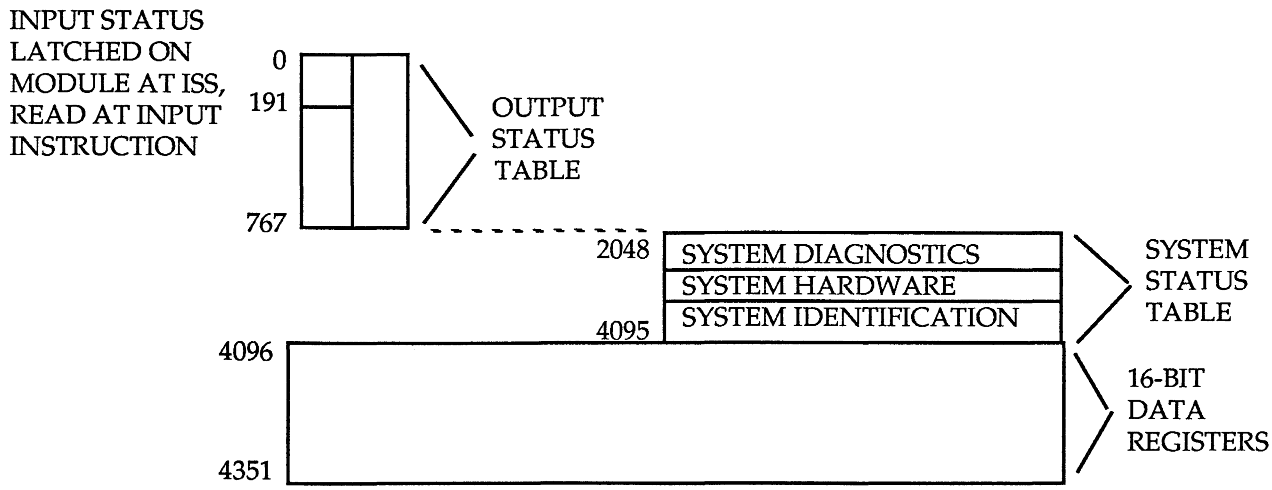


FIGURE 3 - REGISTER MEMORY MAP

A separate portion of the data table is reserved for system status information. This information is categorized as system identification, system hardware and system diagnostics. See SYSTEM STATUS TABLE CONTENTS in the APPENDIX. Input status is stored at the individual input modules and is read by the processor during program execution.

The interface printed circuit board contains the logic circuitry necessary to interface the processor to the rack I/O bus and the option cards. A bank of eight DIP switches enables or disables several functions including: FORCE, battery low start-up inhibit, on-line programming and data change functions. The DIP switch settings determine whether the processor will recognize or ignore processor rack output card faults. Clearing or freezing outputs at recognized card faults is also set at the Interface Board SW1. Refer to the APPENDIX for a complete listing of the Processor Module DIP switches and their functions.

EPROM Memory

An optional non-volatile EPROM memory is available as a redundant user memory backup. Using a commercially available PROM programmer, the user program is transferred from the connected 620-06 to the Loader/Terminal (L/T). The L/T then transfers the program to the connected PROM programmer. The EPROM is then inserted into the socket provided on the PM circuit board. See the APPENDIX for socket location. Refer to the 623-6000 LOADER/TERMINAL USER MANUAL, Form No. 623-8987 or the 623-60 MS-DOS LOADER USER Manual, Form No. 623-8986 for EPROM programming procedures.

The EPROM Programmer must support Motorola "s" record format and contain at least 128K of internal RAM.

PROCESSOR POWER SUPPLY MODULES (PSM)

Model No. 620-0041 (115/230VAC)

The 620-0041 Processor Power Supply is placed in slot I of the 620-06 processor. It may only be used in the full processor rack. The module's front panel contains terminals labeled with A (Line or L1), B (common or L2), and a ground symbol for connecting AC power wiring.

The 620-0041 provides 8 amps of +5VDC power for the modules in the rack. It also supplies 600mA of ±15VDC power for analog I/O operation. Refer to the 620 INSTALLATION MANUAL or CONFIGURATION & ORDERING GUIDE (or individual module specifications) for individual module power requirements.

The maximum normal power consumption of the 620-0041 Power Supply is 95VA. A cold start of this power supply will require a maximum of 15 amps for one cycle.

This power supply is selectable for 115 or 230VAC input by the position of a shorting board located under the module's component cover. The 620-0041 is factory set at 115VAC. The 115VAC selection will allow a voltage range of 85 to 132VAC. The 230VAC

selection allows a 170 to 250VAC range of operation. The frequency of both ranges is 47 to 63 Hz. The PSM offers a front-accessible fuse holder. It is shipped with a 2A Slo-Blo fuse installed for 115VAC operation. The 230VAC 1A Slo-Blo fuse is also shipped with the module. A green LED indicates that 5VDC power is present.

Model No. 620-0083 (85/132 VAC or 170/250 VAC)

The 620-0083 Processor Power Supply may be used with 620-06 Processor. It must be used in a full processor rack and is placed in slot I.

The module front panel contains terminals labeled with A (line or L1), B (Common or L2) and a ground symbol for connecting AC power wiring. The input power for this supply is selectable for either 85-132 VAC or 170-250 VAC.

The 620-0083 provides up to 15 amps of +5VDC power to the rack. It can also provide up to 1.16 amps of $\pm$15 VDC power. Figure 4 shows the relationship between current loads of the ±15VDC source and ±5VDC source. In analog configurations, the 620-0083 provides 10 amps of +5VDC and 1.3 amps of $\pm$15 VDC maximum. The maximum total output power cannot exceed 90 watts. Refer to the 620 INSTALLATION MANUAL (or individual module specifications) for individual module power requirements.

The maximum normal power consumption of the 620-0083 is 110VA. A cold start of this power supply will require a maximum of 20 amps for one cycle.

This power supply is selectable for 115 or 230 VAC input by the position of a toggle switch located under the module's component cover. The 620-0083 is factory set for 115 VAC. The fuse holder is accessible from the front of the module. It is shipped with a Slo-Blo fuse installed for 115 VAC. The green LED indicates that 5 VDC is present.

Model No. 620-0046 (24VDC)

The 620-0046 Power Supply may be used with the 620-06 processor. It may only be used in the full rack and is placed in slot I. The module's front panel contains terminals labeled with +, -, and a ground symbol for connecting DC power wiring.

The 620-0046 provides 8 amps of +5VDC for modules in the rack. It also supplies 600mA of ±15VDC power for analog I/O operation. Refer to the 620 INSTALLATION MANUAL (or individual module specifications) for individual module power requirements.

The maximum power consumption of the 620-0046 Power Supply is 96VA. A cold start of this power supply will require a maximum of 40 amps.

The required input is 20-28VDC with a 24VDC nominal input. This power supply module offers a front-accessible fuse holder and is shipped with an 8A Slo-Blo fuse. A green LED labeled 5VDC is energized when the 5VDC power is present.

Model No. 621-9932 (24VDC)
621-9934 (115/230VAC)

These power supply modules may be used only in the 620-06 processor half-rack or any I/O rack. In a processor half rack they reside in slot G. See the section titled I/O Power Supply Modules for more information on using them in I/O racks.

I/O EXPANDER MODULE (IOEM)

Model No. 620-0053

The I/O Expander Module is an expander module used only in the 620-06 and 620-15 processor full racks. The I/O Expander allows additional I/O to be connected to the 620-06 and 620-15 systems via the 50-pin D connector. Note that the total cable distance in any 620-06 system is limited to 50 feet. No user switch selections are required before installation.

NOTE

An I/O Expander is also required when the processor rack option slot is used.

The 620-0053 I/O Expander Module replaces the 620-0045 version of the same name. See the APPENDIX for more information.

621 I/O SYSTEM

The 621 I/O System is comprised of either 19-inch (full) or 10-inch (half) I/O racks that may house up to 12 or 6 I/O modules respectively. I/O racks are connected to the 620-06 system via a parallel link consisting of a multiconductor cable connecting the processor and I/O to I/O racks, in a daisy chain fashion.

The I/O system includes digital, analog, and special function I/O modules. Refer to the 621 I/O Specifications Manual (Form 620-8995) for individual I/O Module specifications.

621 I/O FULL RACK

Model No. 621-9990

The 621 I/O full rack is identical in size to the 620 processor racks. It houses a maximum of 12 I/O modules, a Parallel I/O Module, and a Power Supply Module.

Model No. 621-9992

The 621 Augmented I/O rack is identical to the 621-9990 I/O rack in size and function. It contains an additional upper bus on the backplane to facilitate communication between modules equipped for dual bus communication (i.e. Servo modules).

621 I/O HALF RACK

Model No. 621-9991

The half rack is approximately 10 inches wide. Useful for installation in narrow enclosures such as motor control centers, it accomodates a maximum of six I/O modules, a Parallel I/O Module, and a Power Supply Module.

I/O POWER SUPPLY MODULES (PSM)

Model No. 621-9932 (24VDC)

The 621-9932 I/O Power Supply is a single width module that provides power for modules within the I/O rack. This module may be used in any I/O rack or processor half rack. The front panel contains terminals labeled with +,-, and a ground symbol for connecting DC power wiring.

It provides 8 amps of +5VDC for the I/O logic circuitry in the rack. It also supplies 600mA of ±15VDC power. Refer to the 620 INSTALLATION MANUAL (or individual module specifications) for individual power requirements.

The maximum power consumption of the 621-9932 is 96VA. A cold start of this power supply will require a maximum of 40 amps.

The required input is 20-28VDC with a 24VDC nominal input. This power supply module offers a front-accessible fuse holder and is shipped with an 8A Slo-Blo fuse. A green LED labeled 5VDC is energized when the 5VDC power is present.

Model No. 621-9933 (115/230VAC)

The 621-9933 I/O Power Supply provides power for modules within the I/O rack. It is a double width module and may be used only in an I/O rack. The modules's front panel contains terminals labeled with A (Line or L1), B (common or L2) and a ground symbol for connecting AC power wiring.

The 621-9933 provides 10 to 15 amps of +5VDC for the I/O logic circuitry in the rack. It also supplies 1.3 to 2 amps of ±15VDC. Figure 4 shows the relationship between current loads of the ±15VDC source and the ±5VDC source. If, for example, the ±15VDC source requires 2 amps, the ±5VDC can draw a maximum of 10 amps. If the ±15VDC requires 1.3 amps, the ±5VDC can draw a maximum of 15 amps. Refer to the 620 INSTALLATION MANUAL (or individual module specifications) for individual module power requirements.

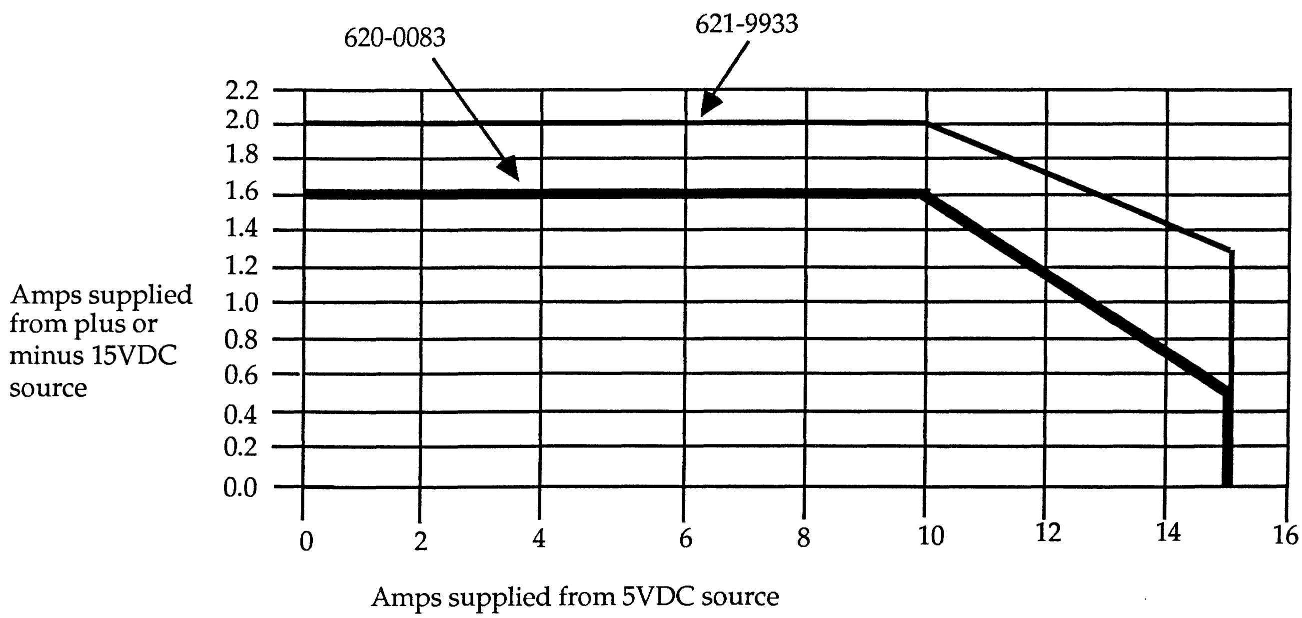


FIGURE 4 - 620-0083 AND 621-9933 POWER SUPPLY DERATING

The maximum power consumption of the 621-9933 Power Supply is 110VA. A cold start of this power supply will require a maximum of 20 amps for one cycle.

The input is selectable for 115 or 230VAC by the position of a toggle switch located under the component cover of the power supply. The 115VAC selection will allow a voltage range of 85 to 132VAC. The 230VAC allows 170 to 250VAC operation. The frequency for both ranges is 47 to 63 Hz. This power supply module offers a front-accessible fuse holder. It is shipped with a 4.0A Slo-Blo fuse installed for 115VAC operation. The 230VAC 2.0A Slo-Blo fuse is also shipped with the module. One green LED, labeled 5VDC, is energized when the 5VDC power is present.

NOTE

> Be sure to match the 115/230VAC toggle switch selection with the corresponding module fuse.

Model No. 621-9934 (115/230VAC)

The I/O Power Supply is a single width module that may be used in any I/O rack or any processor half rack. It provides 8.0 amps of +5VDC power for each I/O rack as indicated by a green LED on the front cover. This module also provides 600mA of ±15VDC power for the operation of analog I/O modules. The power supply is selectable for 115VAC and 230VAC operation by the position of a shorting board located under the component cover of the Power Supply. The frequency for both ranges is 47-63 Hz.

A terminal block at the top of the module's front cover plate is labeled with an A (line or L1), a B (common or L2), and a ground symbol for AC input wiring termination. A front-accessible fuse holder houses a 2 amp Slo-Blo fuse for 115VAC operation. A 1 amp Slo-Blo fuse for 230VAC operation is also shipped.

NOTE

> Be sure to match the 115/230VAC shorting board selection with the corresponding module fuse.

PARALLEL I/O MODULE (PIOM)

Model No. 621-9937

Parallel I/O racks are connected to the processor or other racks using PIOMs. The PIOM controls the I/O rack and communicates with the processor and other PIOMs. The 621-9937 replaces the 621-9930. The 621-9937 must be used in I/O racks that contain any combination of 32-, 16-, and 8-point I/O modules.

The PIOM has two 50-pin D type connectors. The male connector (top) is the IN port and the female connector (bottom) is the OUT port. A green LED labeled ACTIVE illuminates to indicate proper communication from a preceding rack.

Each I/O rack accommodates one PIOM. Different I/O racks within the same system may contain different PIOMs as long as the correct PIOM is used in each rack.

Banks of DIP switches that set the rack configuration, output handling functions, and module configuration by point size, are located on the PIOM printed circuit board. Refer to the APPENDIX for PIOM DIP switch settings.

I/O MODULES

The 621 Universal I/O System offers a variety of 8-, 16-, and 32-point digital modules plus analog and special function modules. Figure 5 presents typical digital I/O modules. See Table 2 for the full listing of 621 I/O modules.

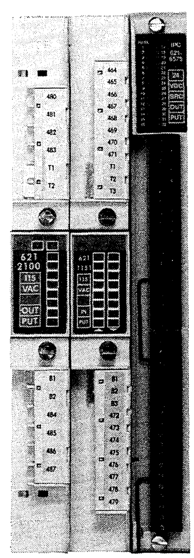


FIGURE 5 - TYPICAL DIGITAL I/O MODULES

The 8- and 16-point modules feature double swing terminal blocks that attach to the rack chassis and fit over the front of the I/O module. The field wiring is split into two small bundles using terminal blocks - one terminal block swings down, closing from the top of the rack, the other swings up, closing from the bottom; both fit over the installed module. The terminal blocks open for easy installation or removal of the circuit board. See Figure 6.

The 8-point terminal block models are factory jumpered at T1 and T2 and B1 and B2. The 16-point terminal block models are factory jumpered at T1, T2, and T3 and B1, B2, and B3. See Figure 7.

The 32-point I/O modules use two 19-position terminal blocks that attach to the front of the I/O Module. The field wiring can be installed in the front of the module using set screws that can be accessed without removing the connector from the module. If a connector must be removed, metal connector bars eject the connectors from the module. See Figure 8.

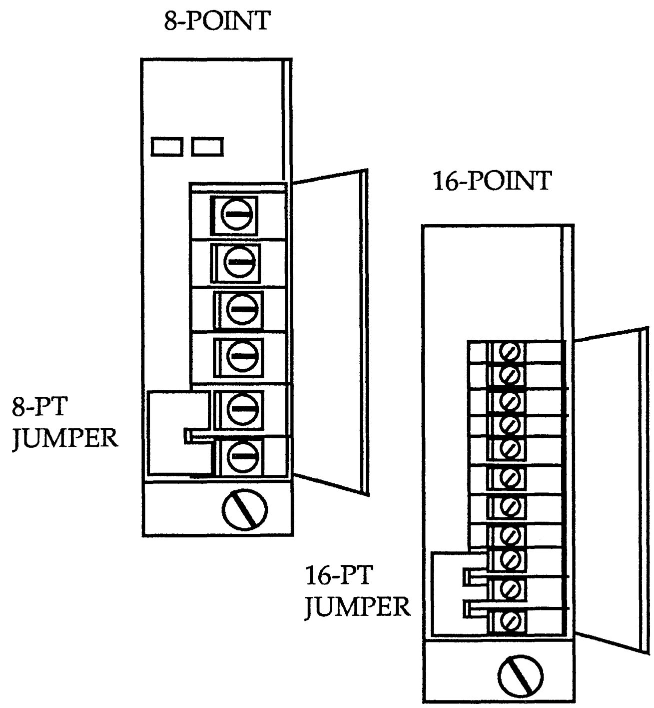


FIGURE 7 - 8-POINT AND 16-POINT TERMINAL BLOCK JUMPERS

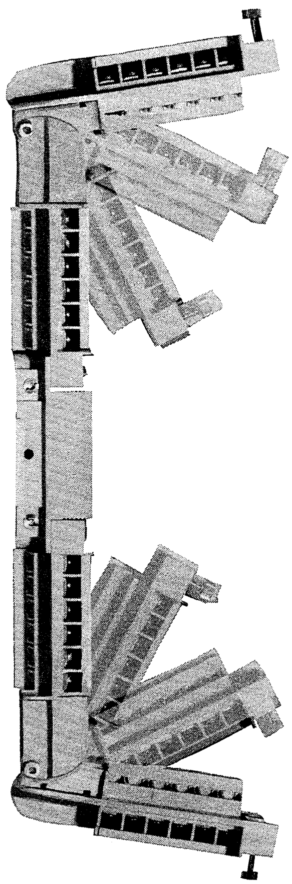


FIGURE 6 - DOUBLE SWING TERMINAL BLOCK

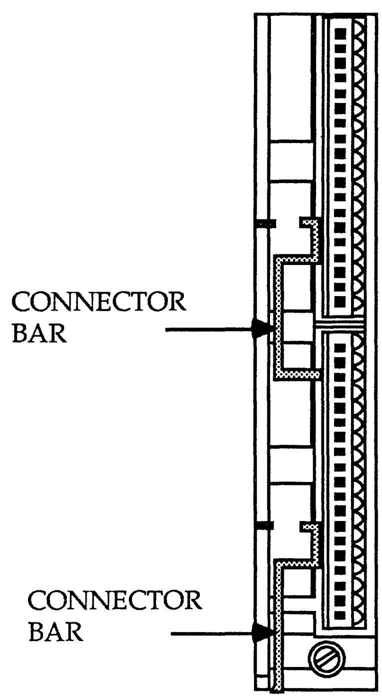


FIGURE 8 - 32-POINT I/O CONNECTOR

TABLE 2- INPUT/OUTPUT MODULES

IPC 621 INPUT MODULES	
MODEL NUMBER	**DESCRIPTION**
621-0009	Simulator Input Module
621-0014	Thermocouple/mV Input Module*
621-0022-A	Isolated Analog Input, 8 pt. (4-20mA)*
621-0022-V	Isolated Analog Input, 8 pt. (0-10V)*
621-1100	115VAC/DC, 8-pt.
621-1101	115VAC/DC Isolated, 6-pt.
621-1151	115VAC, 16-pt.
621-1175	115VAC, 32-pt.
621-1200	230VAC/DC, 8-pt.
621-1201	230VAC/DC Isolated, 6-pt.
621-1500	24VAC/DC, 8-pt.
621-1550	24VAC/DC, 16-pt.
621-3300	5VDC Sink, 8-pt.
621-3450	12VDC Sink, 16-pt.
621-3500	12-24VDC Sink, 8-pt.
621-3502	12-24VDC Sink Fast Response, 8-pt.
621-3550	24VDC Sink, 16-pt.
621-3552	24VDC Sink Fast Response, 16-pt.
621-3575	24VDC Sink, 32-pt.
621-3600	48VDC Sink, 8-pt.
621-3650	48VDC Sink, 16-pt.
621-4300	5VDC Source, 8-pt.
621-4350	5V TTL, 16-pt.*
621-4500	12-24VDC Source, 8-pt.
621-4502	12-24VDC Source Fast Response, 8-pt.
621-4550	24VDC Source, 16-pt.

*Uses PUSH/PULL interface.

TABLE 2 - INPUT/OUTPUT MODULES (CONT.)

IPC 621 OUTPUT MODULES	
MODEL NUMBER	DESCRIPTION
621-0007	Reed Relay, 6-pt.
621-0010-A	Analog Output, 4-pt. (4-20mA)*
621-0010-V	Analog Output, 4-pt. (0-10V)*
621-2100	115VAC, 8-pt.
621-2101	115VAC Isolated, 6-pt.
621-2102	115VAC Source Self-Protected, 8-pt.
621-2150	115VAC, 16-pt.
621-2175	115VAC, 32-pt.
621-2200	230VAC, 8-pt.
621-2201	230VAC Isolated, 6-pt.
621-2500	24VAC, 8-pt.
621-2550	24VAC, 16-pt.
621-6300	5VDC Source, 8-pt.
621-6350	5V TTL, 16-pt.*
621-6450	12VDC Source, 16-pt.
621-6500	12-24VDC Source, 8-pt.
621-6501	12-24VDC Source Self-Protected, 8-pt.
621-6550	24VDC Source, 16-pt.
621-6551	24VDC Low Power Source, 16-pt.
621-6575	24VDC Source, 32-pt.
621-6600	24VDC Source, 8-pt.
621-6650	48VDC Source, 16-pt.
621-6700	120VDC Source (0.5A), 8-pt
621-6701	120VDC Source (2A), 8-pt.

* Uses PUSH/PULL interface.

TABLE 2 - INPUT/OUTPUT MODULES (CONT.)

IPC 621 SPECIAL FUNCTION MODULES	
MODEL NUMBER	DESCRIPTION
621-0004	System Diagnostic Module*
621-0006	BCD Converter*
621-0008	Pulse Input Module*
621-0012	ASCII Communications Module*
621-0016	Controller Access Module*
621-0018	Absolute Encoder Module*
621-0307	High Speed Counter*
621-0576	24VDC 24 Sink In/8 Source Out

*Uses PUSH/PULL interface.

623-6000 LOADER/TERMINAL

The 623-6000 Loader/Terminal is a programming, monitoring and documentation tool used with the 620-06 system as well as the other 620 systems, the 627-70 COP Industrial Microcomputer, and other ASCII peripheral devices. The 623-6000 Loader/Terminal may also be used as a stand-alone 620 program development system. Refer to the LOADER/TERMINAL USER MANUAL (Form 623-8987) for more information concerning 623-6000 operation.

623-60 MS-DOS LOADER

The 623-60 MS-DOS Loader provides another programming option for the 620-06, as well as other 620 systems. This software/hardware package gives any MS-DOS operating system personal computer the capability to program and monitor all IPC 620 programmable controllers. This package can be configured for stand-alone programming operation and allows ladder logic addressing by labels as well as by number. The 623-60 MS-DOS is compatible with the 623-6000 Loader/Terminal ladder logic and documentation. It will read tapes previously made with the L/T, as well as allow the user to write L/T tapes. Enhanced documentation features make the 623-60 MS-DOS an alternative for 620 programming and monitoring.

627 LOCAL OPERATOR STATION (LOS)

The LOS is an industrial MS-DOS AT-compatible workstation for monitoring or supervising a machine or process. It is a hardware platform composed of the user's choice of the following components:

* A powerful processor with MS-DOS 3.21 operating system, large memory, five expansion slots, two serial RS232 ports and one parallel Centronics-compatible parallel port.
* An EGA-compatible industrial monitor
* A 5.25" floppy disk drive
* A 3.5" disk drive
* A keyboard

The LOS provides the functions of the software installed in it. It has a large memory (1M byte RAM) and supports a variety of peripheral devices through five expansion slots, two serial ports and a parallel port. The LOS is used primarily in two ways - as a supervision control system and as an operator interface. More information on the LOS is available in the user manuals: The LOS User Manual (Form No. 627-8980) and the MS-DOS Operating System Manual (Form No. 627-8982).

620-06 SYSTEM CONFIGURATIONS

PROCESSOR MODULE CONFIGURATION

The 620-06 processor module (620-0636) includes three 8-position DIP switches. One is located on the interface pcb; the other two are located on the Microprocessor unit (MPU) pcb. See Figure 13 in the APPENDIX.

SW1 on the interface board determines module response to fault conditions and other processor operations functions. Table 3 in the APPENDIX provide specific switch selection information.

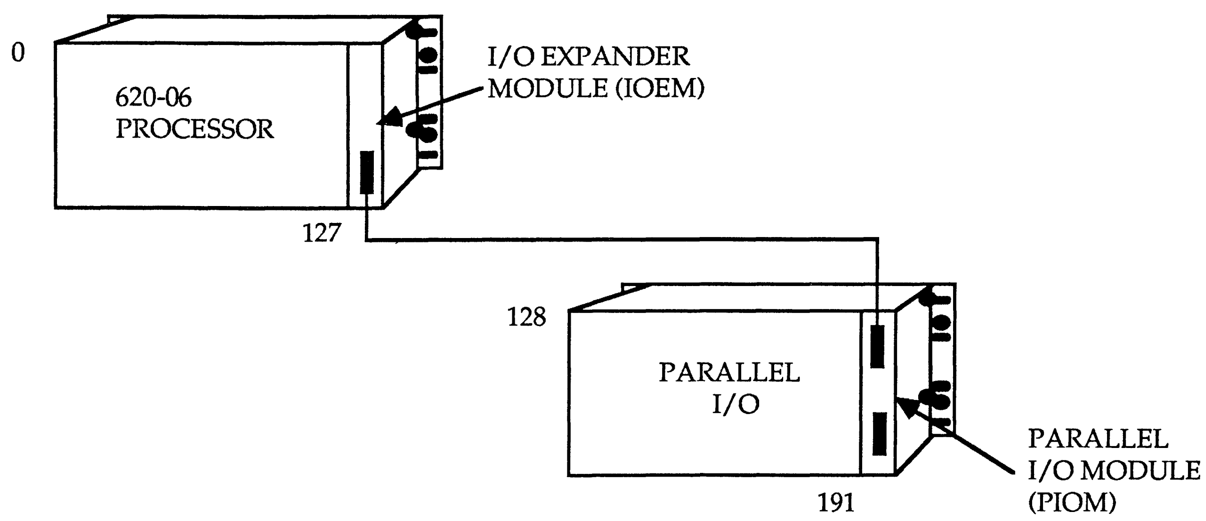
SW 1 and SW2 on the MPU board identify the type of I/O module (0-, 8-, 16-, or 32-point) to be installed in designated processor rack slots. Figure 14 in the APPENDIX provides instructions and examples for configuring processor rack slots.

I/O CONFIGURATION

PARALLEL I/O

Parallel I/O configurations are designed for those applications in which long distances between 621 I/O racks and the processor rack are not required. A maximum of 50 cable feet is allotted for parallel I/O within a 620-06 system.

The I/O Expander Module, is housed within the 620-06 rack and provides a 50-pin D connector. This connector is cabled to one of the two ports on a Parallel I/O Module (PIOM) within the 621 I/O rack. A maximum of two I/O racks may be connected via the PIOM ports in a daisy-chain fashion. The 620-06 offers a maximum of 192 I/O points in a 2K system.



RACK	RACK STARTING ADDRESS	RACK ENDING ADDRESS	I/O POINTS PER SLOT											
			A	B	C	D	E	F	G	H	I	J	K	L
620-06	0	127	8	8	8	8	16	16	32	32	--	--	--	--
I/O#1	128	191	8	8	8	8	16	16	0	0	0	0	0	0

FIGURE 9 - EXAMPLE PARALLEL I/O CONFIGURATION

ADDRESSING

The 620-06 processor rack may house up to eight I/O modules. The module in processor rack slot A always receives the starting address of zero. The starting address must be set for each I/O rack in a parallel I/O system, and each I/O slot must be set for 0, 8, 16, or 32 addresses. Both the starting address and the address configuration are selected using DIP switches on the PIOM. Each additional I/O rack starting address should be set to the ending address of the previous I/O rack plus one (Figure 9).

NOTE

The starting address of any PIOM MUST be higher than the highest address allotted to the previous processor rack.

Each I/O slot is normally set for the type of I/O module to be installed in the slot (i.e. 8 addresses assigned to a slot that will contain an 8-point I/O module). Slots can be set for more addresses than the installed module (i.e. 32 addresses assigned to a slot that will contain a 16-point module). Zero can be assigned to a slot when necessary as for double width modules.

SETTING 621-9937 PIOM DIP SWITCHES

PIOM DIP switch bank locations are shown in the APPENDIX in Figure 5 and settings are defined in Table 4. Follow this procedure when setting PIOM DIP switches.

1. Determine the starting address of the rack by adding a one to ending address of the previous rack.

2. Set the rack starting address using DIP switch bank SW1. Each switch position of SW1 is assigned a value as follows:

DIP SWITCH POSITION	VALUE
1	8
2	16
3	32
4	64
5	128
6	256
7	512
8	1024

NOTE

The starting address of the last rack in the system may not be higher than 184.

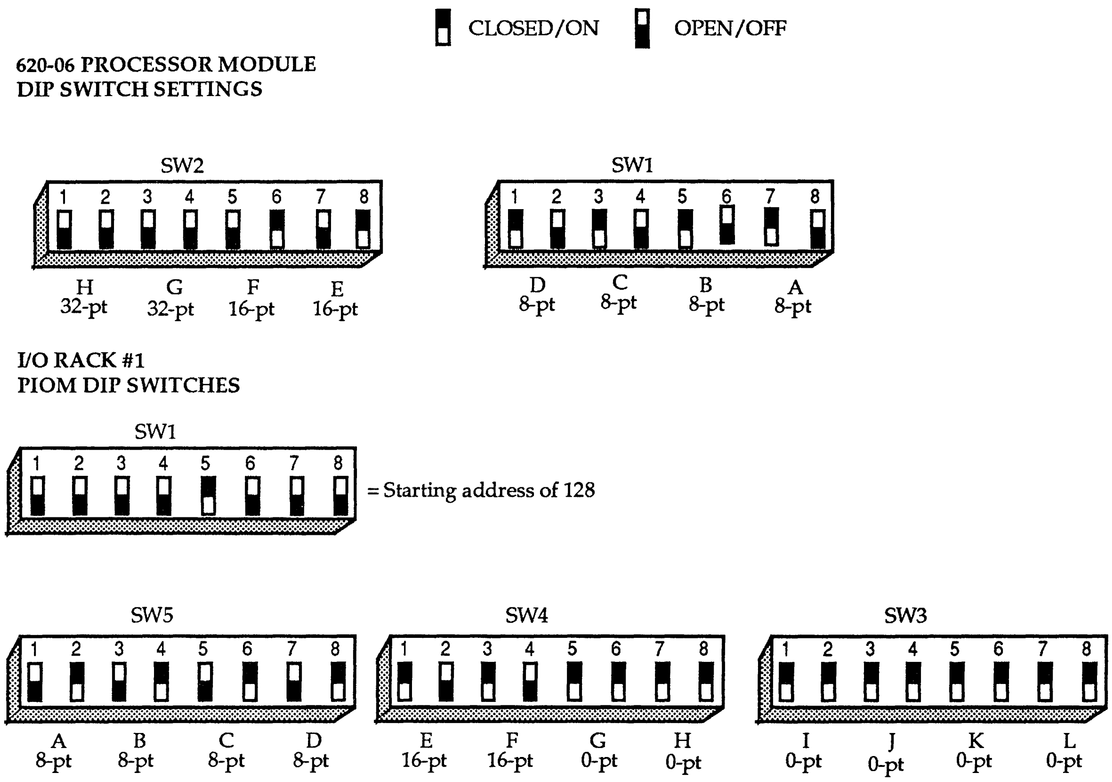


FIGURE 10- EXAMPLE DIP SWITCH SETTINGS

Closing a switch position adds that value to the starting address of the rack. For example, if position 1 and 4 in the SW 1 switch are the only closed positions, the starting address of the rack will be 72 (8 + 64).

3. Determine the desired rack output states if an output fault should occur. Switch SW2, positions 1 and 2 control this function. Refer to Table 4 in the APPENDIX.

4. Assign a number of I/O addresses for each slot in the rack. Figure 16 in the APPENDIX describe which DIP switch positions in banks SW3, SW4, and SW5 set the addresses for each rack slot.

NOTE

Modules with 8-, 16-, and 32-points may be mixed within the same rack; however, the proper DIP switches on the Parallel I/O Module must be set for each slot in the I/O rack.

Figure 10 shows the 621-9937 PIOM DIP switch settings for the example parallel configuration from Figure 9.

NETWORK CONFIGURATIONS

CONTROL NETWORK

A Control Network is a high speed peer-to-peer communications system in which as many as eight PCs can share I/O status over a serial link. Field start-up time is greatly reduced using this communication method since it eliminates wiring I/O between PCs. The Control Network Module (CNM) connects to the processor bus and allocates 256 I/O status bits or 16 registers for its use. These status bits or registers are designated for receiving I/O status or data from other 620 processors on the network. The CNM also transmits processors I/O status (32 or 64 bits) to other 620 processors on the link. All eight CNMs on a Control Network are serviced within 18ms.

The link is a single twisted pair cable with a maximum length of 4000 feet. If the optional twin-axial cable is used, the maximum cable length is expanded to 8000 feet. Control Network Modules are connected to the link in a multi-drop configuration as seen in Figure 11.

Refer to the CONTROL NETWORK INTRODUCTION/USER MANUAL (Form 620-8994) for additional CNM information.

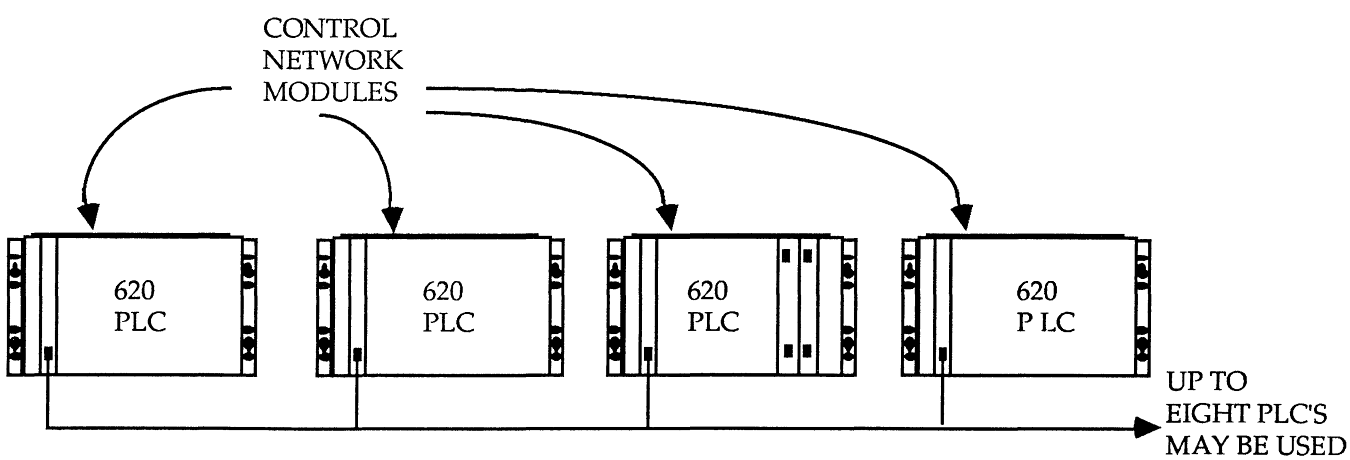


FIGURE 11 - EXAMPLE CONTROL NETWORK CONFIGURATION

620-06 THEORY OF OPERATION

PROCESSOR MODES OF OPERATION

The three-position keyswitch on the front panel of the 620-06 Processor Module determines the mode of operation. The three operating mode features in the 620-06 are PROGRAM, DISABLE, and RUN/PROGRAM.

PROGRAM MODE

The system may be placed in the PROGRAM mode using the front panel keyswitch, the 623-6000 Loader/Terminal or a Communications Interface Module (CIM). When the system is in the PROGRAM mode, the Processor Module receives commands from the Loader/Terminal or CIM and executes only those commands. The user may clear, enter and edit the ladder diagram program in this mode. The user program is not scanned nor is I/O updated.

PROGRAM Mode System Status

While the 620-06 is in the PROGRAM mode, the RUN LED is turned OFF and the scan loss timer is cleared. All local I/O are cleared or frozen according to the DIP-switch settings of the PIOMs. FORCE functions are possible if the FORCE enable switch on the processor is enabled. Timer and counter values may be modified regardless of the setting of the data-change DIP switch on the processor.

For the processor to be changed from the PROGRAM mode to any other mode of operation, the keyswitch must be changed to one of the other modes and all software requests for PROGRAM mode must be cleared. Software requests may be made from the Loader/Terminal or from a CIM. If the processor is placed in the PROGRAM mode by a software request and the request is cleared, the processor returns to the mode identified by the keyswitch position.

DISABLE MODE

When the keyswitch is in the DISABLE position, the processor executes the ladder logic program as it does in the RUN mode. However, the processor does not update real output points in the system; it updates only outputs in the output status table. The DISABLE mode is the default mode. If the processor does not detect another mode, it defaults to this mode.

DISABLE Mode System Status

While the processor is in the DISABLE mode, the RUN LED is turned ON. The scan loss timer is cleared at the beginning of every PLC scan unless a timeout occurs. If a timeout occurs, the RUN LED is turned OFF.

All local I/O are cleared or frozen according to the DIP switch settings on the processor board. The hardware of the processor module sends a power fail signal to the I/O system. Outputs are cleared or held in the last state in the DISABLE mode, depending on the PIOM setting for each I/O rack and the processor module DIP switch selections.

FORCE functions are permissible if they are ENABLED by the processor DIP switches. Timer and counter modifications may be made.

To change the processor from the DISABLE mode to any other mode of operation, one of the following conditions must be met: 1) the keyswitch is changed, 2) the Loader/Terminal generates a request for Software Program Mode, 3) a CIM generates a Software Program Mode request, or 4) the processor fails diagnostics and defaults to the Diagnostics Fail Mode.

RUN/PROGRAM MODE

When the keyswitch is in the RUN/PROGRAM position, the processor is capable of being placed in the RUN mode or the PROGRAM mode.

RUN Mode in RUN/PROGRAM

The system is in the RUN mode when the front panel keyswitch is in the RUN/PROG position and all of the following conditions are met: 1) requests for Software Program Mode from the Loader/Terminal or a Communication Interface Module are not present, and 2) all diagnostic tests have been passed. The RUN mode is the main control mode for the processor.

The processor performs a self-test when it enters the RUN mode. After the self-test, the system executes a retentive scan and all non-retentive outputs from 0 to 767 are turned OFF. Retentive outputs retain the state of the last scan prior to being taken out of the RUN mode.

After the retentive scan is complete and the processor verifies that ISS and End of Memory (EOM) reside in the user program, the Input Status Scan (ISS) begins. The processor strobes every input module to latch the data present at each input when the strobe is momentarily applied. At the same time, the processor examines output card faults. If any output card faults are detected in the I/O system, the fault information is inserted in the System Status Table. The ISS operation takes approximately 2 milliseconds to execute.

The processor then reads and executes the second memory location and continues through the user program. Outputs are updated at the instant the associated output is solved. A Return to Beginning of Program or End of Memory instruction causes the scanning sequence to repeat. In this instance, a Return to Beginning of Program is an optional instruction programmed by the user. The EOM instruction is automatically deposited into the user memory at the end of the user program. The ISS instruction is automatically deposited in the first memory location of the user memory.

RUN Mode System Status in RUN/PROGRAM

While the processor is in the RUN mode, the RUN LED is turned ON. The scan loss timer is cleared at the beginning of every PLC scan unless a timeout occurs. If a timeout occurs, the RUN LED is turned OFF.

All local I/O are cleared or frozen according to the DIP-switch settings on the processor board. They are cleared if one of the following types of faults are detected: 1) a local I/O card fault, 2) an external power failure, 3) a process scan loss, 4) a processor change to either the PROGRAM or DISABLE mode. They are frozen if one of the following types of faults are detected: 1) an external power failure, 2) a process scan loss, 3) a processor change to either the PROGRAM or DISABLE mode.

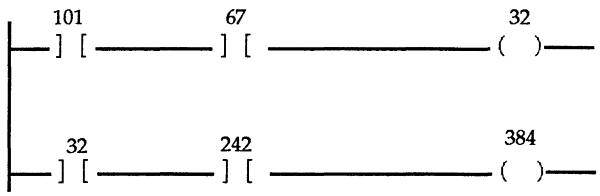
FORCE functions are permissible if they are ENABLED by the processor DIP switches. Timer and counter modifications may be made and Augmented RUN Mode Programming may be used if the data-change function is ENABLED on the processor DIP switches.

To change the processor from the RUN mode to any other mode of operation, one of the following conditions must be met: 1) the keyswitch is changed to one of the other modes, 2) the Loader/Terminal generates a request for Software Program Mode, 3) a CIM generates a Software Program Mode request, or 4) the processor fails diagnostics and defaults to the Diagnostics Fail Mode.

Program Execution Sequence

Assume that the processor has now completed the ISS and is ready for the actual program execution.

Using the sample program in Figure 12, represented by the following logic lines, program execution would be as follows:



1. The first instruction (-] [-, 101) is read from memory causing a logical OR to be performed on the binary digit stored at address 101 in the Output Status Table of the processor and the binary digit read from the I/O card. Assuming that input contact 101 is closed, a binary 1 is read from the I/O card at address 101. All non-retentive Output Status Table bit addresses are cleared to zeroes during retentive scan, so the OR operation will result in a 1 (input contact 101 closed).

2. The next instruction (-] [-, 67) is brought from memory and a logical OR performed on the I/O point and the Output Status Table at address 67. Assuming that input contact 67 is closed, a binary 1 is read from the I/O card at address 67.

3. The next instruction (-( )-, 32) is brought from memory. The processor recognizes that output 32 must be turned ON since both input contacts 101 and 67 are closed. The processor transmits a signal via the field I/O bus to energize output 32 and also posts a binary 1 in bit address 32 of the Output Status Table.

4. The next instruction (-] [-, 32) is brought from memory and a logical OR is performed on the I/O point and the Output Status Table at address 32. Bit address 32 on the I/O card is read as 0, but a binary 1 was just posted at address 32 in the Output Status Table as a result of the previous instruction. The result of the logical OR is a binary 1 (contact 32 closed).

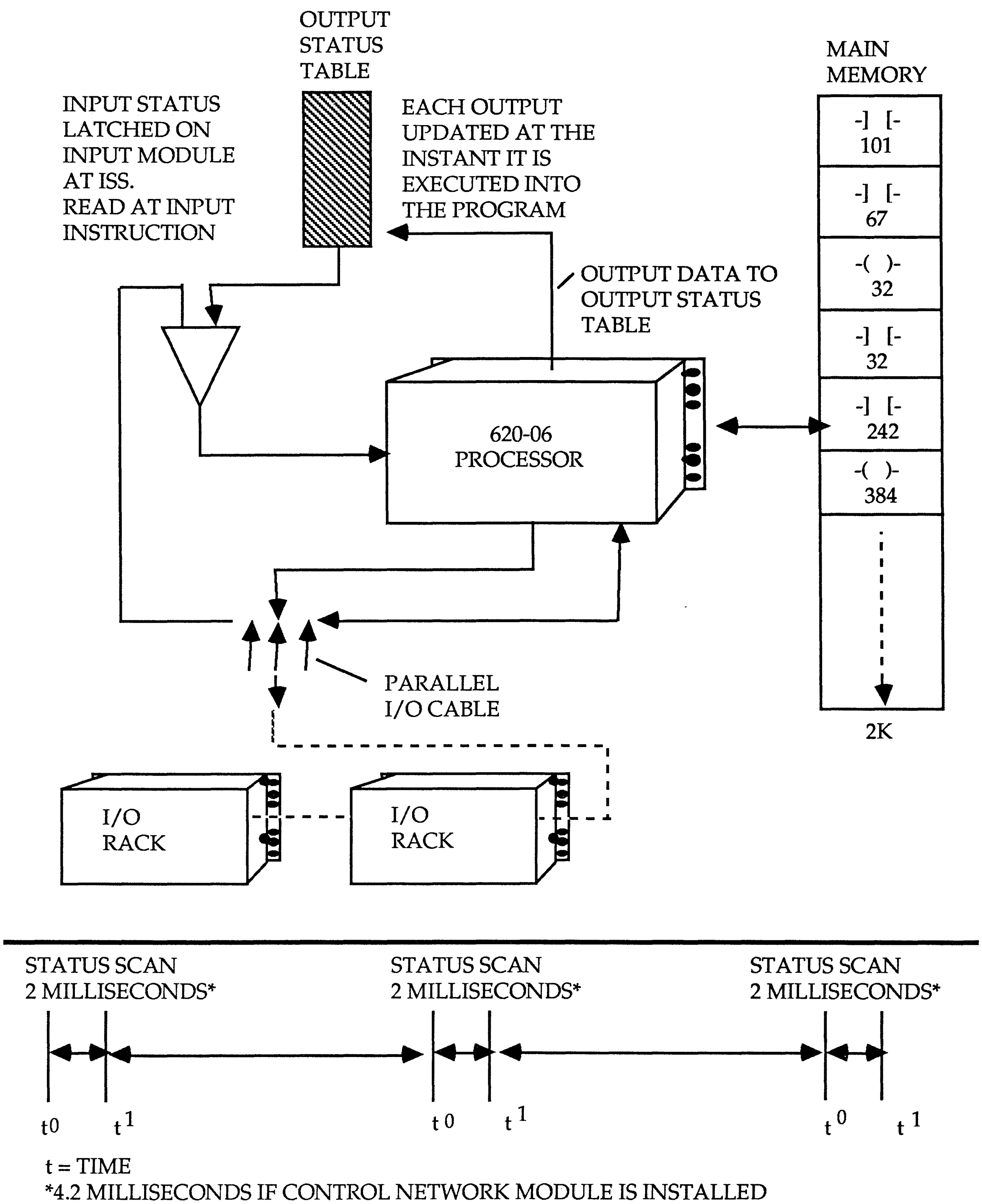


FIGURE 12 - 620-06 PROGRAM EXECUTION

5. The next instruction (-] [-, 242) is brought from memory and a logical OR performed on the I/O point and the Output Status Table at address 242. Assuming that input contact 242 is open, 0 is read from the I/O card at address 242.

6. The next instruction (-( )-, 384) is brought from memory. The processor recognizes that contact 32 is closed, but contact 242 is open; therefore, output 384 must be de-energized. The processor transmits the signal via the field I/O bus to de-energize output address 384 and posts a 0 in bit address 384 of the Output Status Table.

7. The remainder of the instructions are executed until the End of Memory instruction is reached. The EOM returns the program execution sequence. The first memory word of the program, ISS and the other beginning of memory routines are run.

PROGRAM Mode in RUN/PROGRAM

To enter the PROGRAM mode while the keyswitch is in the RUN/PROGRAM position, the processor must receive a Software Program Mode request from the Loader/Terminal or from a CIM.

While in the PROGRAM mode of the RUN/PROGRAM position, the processor operates in the same manner described in the section entitled "PROGRAM MODE".

AUGMENTED RUN MODE PROGRAMMING (ARMP)

ARMP is included with all 620-06 processors that have a firmware revision of 48 or greater.

Through Augmented RUN Mode Programming, ladder logic changes, such as additions, deletions and other editing, may be made to the user program during execution. This does not affect the program being executed except to increase the scan time by a maximum of 20 milliseconds. To execute ARMP functions, the following conditions must be met: 1) the processor must be a Rev 48 or higher, 2) the processor must be in the RUN/PROG mode, 3) the processor must have on-line programming enabled, 4) the processor must have the watchdog timer set for at least 20 milliseconds above the normal scan time, 5) the Loader/Terminal must be using MS-DOS 3.0 or higher, and 6) the Loader/Terminal must be placed in the PROGRAM mode.

A CIM may not write to memory while the processor is peforming an ARMP function. The user should monitor the System Status Tables to determine when the ARMP function is not in effect and then conduct memory write functions. System Status Table registers 2487 and 2488 are updated by the processor so that the CIM user may monitor ARMP functions in progress. These registers contain hex AAAA (43,690) when ARMP is in progress and hex 5555 (21,845) when ARMP is not in progress.

NOTE

Refer to the MS-DOS Loader Manual 3.0 (Form No. 623-8986) for ARMP procedures.

PRIORITIES FOR SELECTING PROCESSOR MODE

Under most circumstances the processor keyswitch determines the processor mode of operation. However, some CIM and Loader/Terminal functions can override the keyswitch and change the mode of operation. The modes of operation are prioritized in the following order from highest to lowest: 1) RUN/PROGRAM, 2) DISABLE, 3) PROGRAM.

A CIM cannot place the processor in a mode higher in priority than the one designated by the processor keyswitch, but it can place it in a mode lower in priority. The Loader/Terminal can place the processor only in the PROGRAM mode and return the processor to the mode designated by the processor keyswitch. In situations where the CIM and the 623 Loader/Terminal are trying to control the processor mode at the same time, the Loader/Terminal has priority.

EPROM OPERATION

The following EPROM OPERATION description applies to Firmware Revision Level 48 or higher using the 27128 EPROM.

The 620-06 Processor may be fitted with an optional EPROM memory in MPU socket U32 for permanent user program storage. Processors with an EPROM memory installed transfer user EPROM memory to RAM during the processor power-up cycle. During this cycle, the processor determines whether the battery level was sufficient to have retained user RAM memory, Register Table data and retentive instruction data while the processor power was removed. The processor also determines whether the powerup cycle is a warm or cold start (initial power up).

If the power-up cycle is a cold start, or a low battery condition is detected, the following occurs:

1. User program EPROM contents transferred to RAM.

2. Output Status Table cleared to zero (addresses 0-767).

3. Register Table data transferred from EPROM to the Register Table (addresses 4096-4351).

4. Jump Table (for NSKR instructions with addresses 8192-8447) transferred.

If the power-up cycle is a warm start, and a good battery condition is detected, the following occurs:

1. User program EPROM contents transferred to RAM.

2. Neither the Output Status Table nor the Register Table is cleared to zero. Both tables retain the data from the last processor scan.

3. Jump Table not transferred.

This procedure allows retentive instructions (Retentive Outputs and Send Outs) to operate correctly during processor power outages. Timer and counter accumulated values are also saved during power-down conditions.

When program changes are made to the EPROM memory, it is recommended that the battery be removed for 1 minute before re-powering the system. This will ensure that a cold-start power up is performed.

When the EPROM is installed, the processor will not allow the Loader/Terminal or Communications Interface Module to make program changes in the RAM memory in ANY processor mode. The only functions allowed are the following:

1. Changes to data residing in the Register Table. This includes timer and counter presets and accumulated values, and Bring In and Send Out instructions.

2. Changes to program title and date in the System Status Table.

3. Force functions.

PARALLEL I/O OPERATION

The 621 parallel I/O system consists of one or more I/O racks. The first rack is connected from the I/O Expander Module (IOEM) in the processor rack to the PIOM in the I/O rack. Subsequent racks are connected from I/O rack PIOM to PIOM in a point-to-point (daisy-chain) configuration. A maximum of two PIOMs may be connected. Communication takes place over a parallel bus of multiconductor cables connecting the IOEM in the processor rack and the PIOMs in the I/O racks.

NOTE

Although the 620-06 can accommodate up to five I/O racks, using the maximum number of I/O (192) requires only two external racks if all processor and I/O rack slots are filled with 8-point I/O.

OPERATION OVERVIEW

1. During processor Input Status Scan (ISS), the processor momentarily stops solving the control program to latch data present at the input cards. The ISS automatically occurs before every program scan or during program control when the ISS instruction is encountered.

2. During the ISS, the processor systematically generates I/O module address data, which is transmitted to all PIOMs on the parallel link.

3. PIOMs decode the address data and in turn generate card selects to all I/O cards in the I/O rack.

4. After an input module receives a card select, the data present at each input is latched on the input module.

5. At this point, output modules are queried for card faults. The processor can store the locations of up to eight card faults. The most significant address of the faulted I/O module is stored in the System Status Table.

6. By the end of the Input Status Scan, the status of all inputs has been recorded in the Holding Registers on the input cards.

7. The processor then commences program execution. As input instructions are solved, the processor reads the input data from the input module. As output instructions are solved, the processor posts the status of the output instructions in the Output Status Table.

8. The processor transmits the address data and output status to the I/O system; the PIOMs decode the address information and generate a card select to the appropriate output module.

9. After the output module is selected, a strobe command allows the output to turn ON or OFF, depending on the output command.

10. The 620-06 processor also performs a diagnostic function with every output command. When an output instruction is solved, the address data and output status, and the complement of this informaton, is sent to the I/O system. These two groups of data are transmitted to the appropriate output module on separate data lines. At the output module, a comparison between the data and its complement is made. If a miscompare occurs signifying a module or I/O bus fault, the output module sets a fault flag. This flag is read by the processor during Input Status Scan. The address of the faulted module is then posted in the System Status Table.

PARALLEL I/O SHUTDOWN

The parallel I/O system will halt its operation under the following conditions:

1. The processor sends a power fail signal to the PIOMs located in the I/O racks when the processor is in the PROGRAM or DISABLE mode or when processor scan loss occurs. The PIOMs, upon receiving the power fail signal, either turn all outputs OFF or hold outputs in their last state (depending on the selected DIP-switch setting) until the power fail signal is removed. The Processor Module performs the same function for processor rack I/O modules.

2. If the power supply in the processor rack or an I/O rack detects that the AC power supply is less than 83 volts in 115VAC operation or 166 volts in 230VAC operation for longer than 11.5 milliseconds, the power supply sends a power fail signal to the other I/O racks and to the Processor Module. The outputs in the other racks clear or freeze, depending on the response selected via DIP switches, and the processor halts operation. Note that the power fail level for 24VDC operaton is 19 volts with a power fail delay of 7 milliseconds.

3. The PIOMs and the Processor Module can be individually selected to recognize output module faults occuring in their racks. If faults are to be recognized and acted upon, the PIOM or Processor Module will clear or freeze outputs in its rack only.

PROCESSOR DIAGNOSTICS

The 620-06 processor self-diagnostics enable the user to locate system faults at the module level. These troubleshooting aids are designed to reduce service time and increase up-time. LED indicators signify the occurrence of system faults directing the user to fault locations. Most system faults can be repaired by replacing a single module. The self-diagnostic tests are conducted in a series that begins with the Processor Module, and proceeds through the processor backplane and other modules within the processor rack. The diagnostics are divided into four categories: power-up self-test, program memory check, on-line checks, and Loader/Terminal diagnostics.

POWER-UP SELF-TEST

The Processor Module (PM) begins executing the self-diagnostic test program stored in the executive ROM. Power-up steps are as follows:

1. Test data flow through microprocessor and operation of microprocessor register.

2. Compute checksum of executive ROM.

3. Test Read/Write ability of Processor Module working module.

4. Check chip selects to every RAM to ensure all memory can be addressed.

5. Test Read/Write ability (non-destructive) of Processor Module memory used for register storage and system status.

6. Test Read/Write ability (non-destructive) of user memory and size of user memory.

7. Test Read/Write ability of Output Status Table (non-destructive).

If the 620-06 fails the RAM memory test during power-up self-test, power down the system and remove the battery. This clears the test fail flag and enables restart.

PROGRAM MEMORY CHECK

The user program memory is checked through a comparison of checksum calculations. If any on-line changes occur, the initial checksum is recalculated. The checksum calculation and comparison check is as follows:

1. The processor calculates the initial checksum of the user program during the retentive scan.

2. The processor calculates checksum of user program while program is running by reading 24 memory words per scan. If any on-line changes occur, the processor starts over by recalculating the initial checksum.

3. If the two checksum calculations match, no error has been detected.

4. If the two checksum calculations do not match, the processor sets the error flag and stops scanning. See the MS-DOS Loader Manual 3.0 (Form No. 623-8986) for a complete list of System Status Table registers.

ON-LINE CHECKS

On-line checks are functional tests performed at the beginning of every scan, before inputs are updated.

1. Test for an Input Status Scan instruction in the first user memory location.

2. Test for End of Memory instructions in proper places in the user program.

3. Reset scan loss timer (Scan loss time delay: 150 milliseconds min., 200 milliseconds max.)

If any of these steps fail, the processor immediately goes into the complete self-test. The output modules also check for proper data flow during the program scan as described in Step 10 of the PARALLEL I/O OPERATION OVERVIEW.

MONITORING DIAGNOSTICS

The 623-6000 Loader/Terminal allows the user to examine the results of processor diagnostics. PLC hardware and software status may be accessed and monitored using the Loader CRT.

The HARDWARE STATUS display provides the user with data concerning processor revision and Test Status, program scan time, status of DIP-switch-selected options and force count.

The second display is SELF-TEST, which indicates pass/fail status of the individual hardware elements involved in the self-test routine. If during a PLC Diagnostic Fail, the processor has passed in the SELF-TEST display and SELF-TEST FAIL (STF) appears in the Loader edit line, this indicates a software error. To correct this error, clear the program memory and reload the program.

The I/O MODULE STATUS display lists the total I/O module faults at any given time and the most significant addresses of up to eight faulted modules.

APPENDIX

PROCESSOR MODULE DIP SWITCHES

Table 3 and Figure 13 are references for model number 620-0636.

TABLE 3 - PM INTERFACE BOARD DIP SWITCH SETTINGS

SWITCH	POSITION	STATE	FUNCTION
SW1	1	Closed/ON[1]	Clear rack outputs when a fault is detected [2]
		Open/OFF	Freeze rack outputs upon fault detection[3]
	2	Closed/ON[1]	Recognize rack output faults; respond per Switch 1
		Open/OFF	Ignore rack output faults
	3		Not Used
	4	Closed/ON[1]	Enable Force function
		Open/OFF	Disable Force function
	5	Closed/ON[1]	Enable on-line programming and data change
		Open/OFF	Disable on-line programming and data change
	6	Closed/ON[1]	Enable startup inhibit with low battery
		Open/OFF	Disable startup inhibit with low battery
	7	Closed/ON[1]	Enable scan loss timer
		Open/OFF	Disable scan loss timer
	8	Closed/ON[1]	Clear I/O during software program mode
		Open/OFF	Freeze I/O during software program mode

[1] Factory Setting

[2] Fault is defined as 1) Recognized card fault, 2) External power fail, 3) Processor scan loss, 4) PROGRAM or DISABLE mode

[3] Fault is defined as: 1) External power fail, 2) Processor scan loss, 3) PROGRAM or DISABLE mode

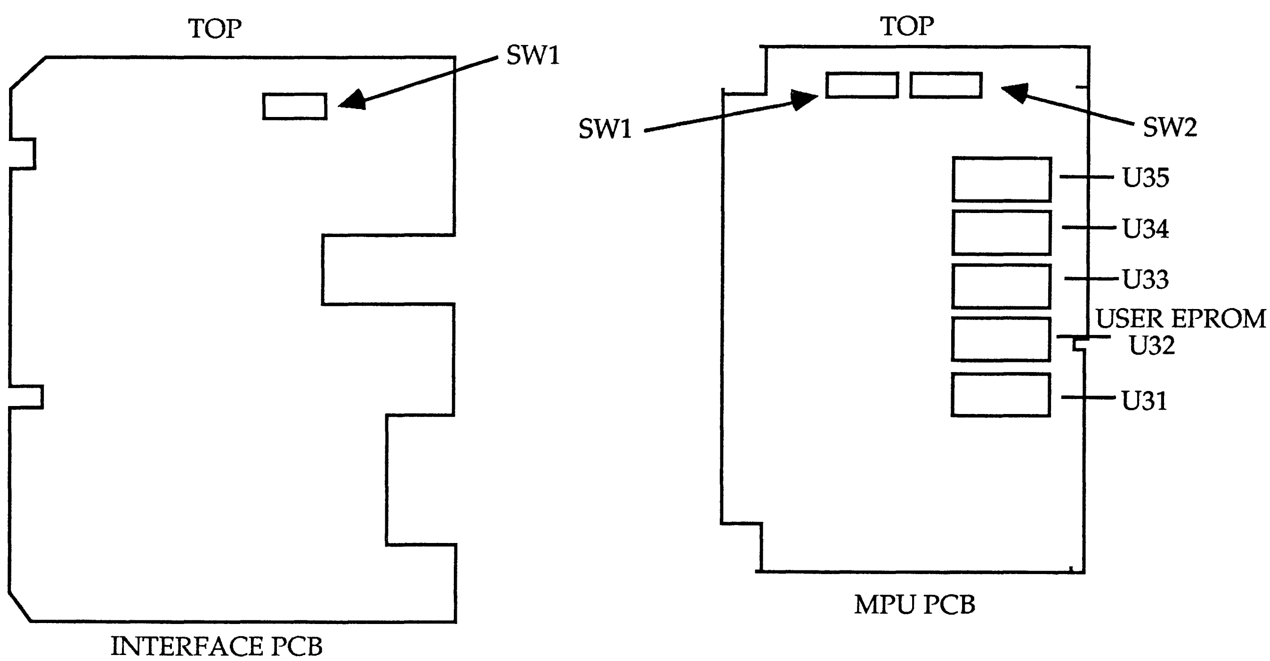


FIGURE 13 - PROCESSOR MODULE DIP SWITCH LOCATIONS AND EPROM SOCKET LOCATION

CONFIGURING PROCESSOR RACK SLOTS

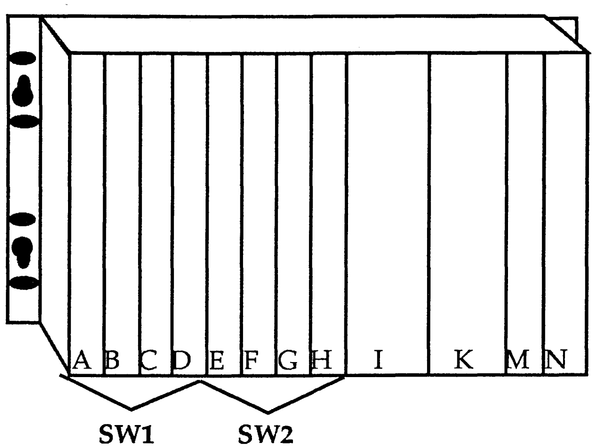
The following procedure describes how to set the point capacity of each I/O slot in the Processor Rack. Processor Board switches SW1 and SW2 are referenced. Refer to Figure 14 while using this procedure.

1. Locate the desired slot by slot letter.

2. Find the DIP switch bank (SW1 or SW2) that contains the desired slot letter. The corresponding slot letter is silkscreened on the circuit board.

3. Find the pair of DIP switch positions that control the slot's configuration. There are two numbers, a "1" and a "2", silkscreened on the circuit board for each DIP switch pair. Notice that for each DIP switch pair, one switch position is designated as the First Setting (labeled 1) and the other is designated as the Second Setting (labeled 2). For example, slot C is configured by the SW1 DIP switch positions 4 and 3 (position 4 is the First Setting and position 3 is the Second Setting).

4. Refer to Figure 14, SLOT CONFIGURATION SELECTION table. This table lists the settings for 0-8-, 16- and 32-point selection. Find the desired point requirements in the table and set the corresponding DIP switch positions.

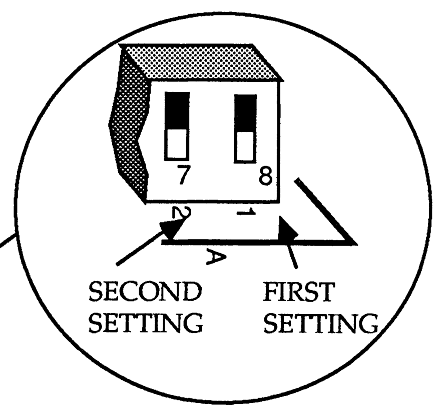


I POWER SUPPLY MODULE

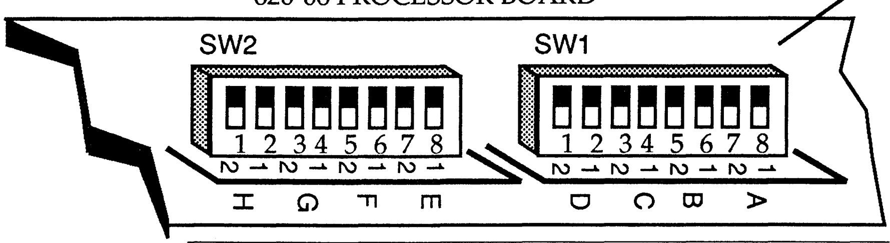
K 620-06 PROCESSOR MODULE

M BLANK SLOT FOR OPTION MODULE

N I/O EXPANDER MODULE



620-06 PROCESSOR BOARD



SETTINGS are silkscreened on Circuit Board: 1 is First Setting, 2 is Second Setting. The table below explains slot configurations using switch SETTINGS.

SLOT CONFIGURATION SELECTION

MODULE TYPE	SETTING FIRST	SETTING SECOND
0-Point	Closed/ON	Closed/ON
8-Point	Open/OFF	Closed/ON
16-Point	Closed/ON	Open/OFF
32-Point*	Open/OFF	Open/OFF

*Factory Setting for all switches

Example:
- Slot B with a 16-point module
  - SW1, position 6 -Closed/ ON
  - SW1, position 5 - Open/OFF
- Slot G with an 8-point module
  - SW2, position 4 - Open/OFF
  - SW2, position 3 - Closed/ON

FIGURE 14 - SETTING PROCESSOR MODULE DIP SWITCHES

TABLE 4 - 621-9937 PIOM SW1 AND SW2 DIP SWITCH SETTINGS

SWITCH	POSITION	STATE	SWITCH VALUE	
SW1	1	Closed/ON	8	Determines starting address for the parallel I/O rack (e.g. closing positions 2, 4, and 6 yields a starting address of 16+64+256=336)
		Open/OFF[1]	0	
	2	Closed/ON	16	
		Open/OFF[1]	0	
	3	Closed/ON	32	
		Open/OFF[1]	0	
	4	Closed/ON	64	
		Open/OFF[1]	0	
	5	Closed/ON	128	
		Open/OFF[1]	0	
	6	Closed/ON	256	
		Open/OFF[1]	0	
	7	Closed/ON	512	
		Open/OFF[1]	0	
	8	Closed/ON	1024	
		Open/OFF[1]	0	
SW2	1	Closed/ON[1]	Clear outputs with 1) switch 2 closed and I/O fault occurs, 2) external cable disconnect, 3) external power failure, 4) processor in PROGRAM or DISABLE modes	
		Open/OFF	Outputs remain the same; with the above conditions	
	2	Closed/ON	Recognize an output module fault	
		Open/OFF[1]	Ignore an output module fault	
	3		Not used	
	4		Not used	

[1] Factory setting

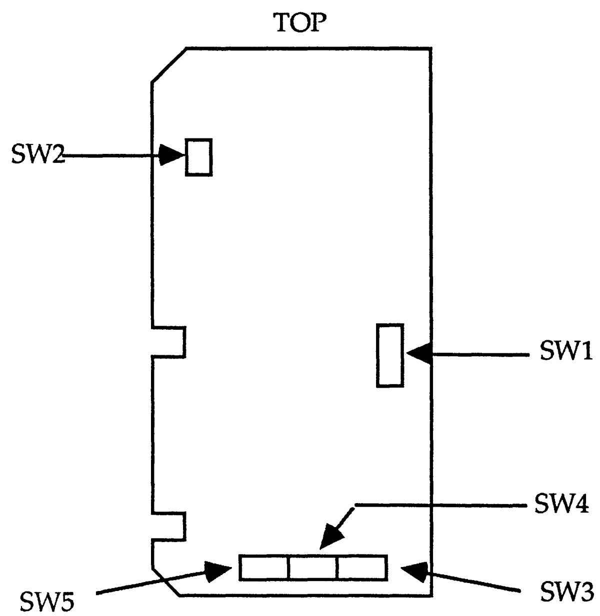


FIGURE 15 - 621 - 9937 PIOM DIP SWITCH LOCATIONS

CONFIGURING I/O RACK SLOTS

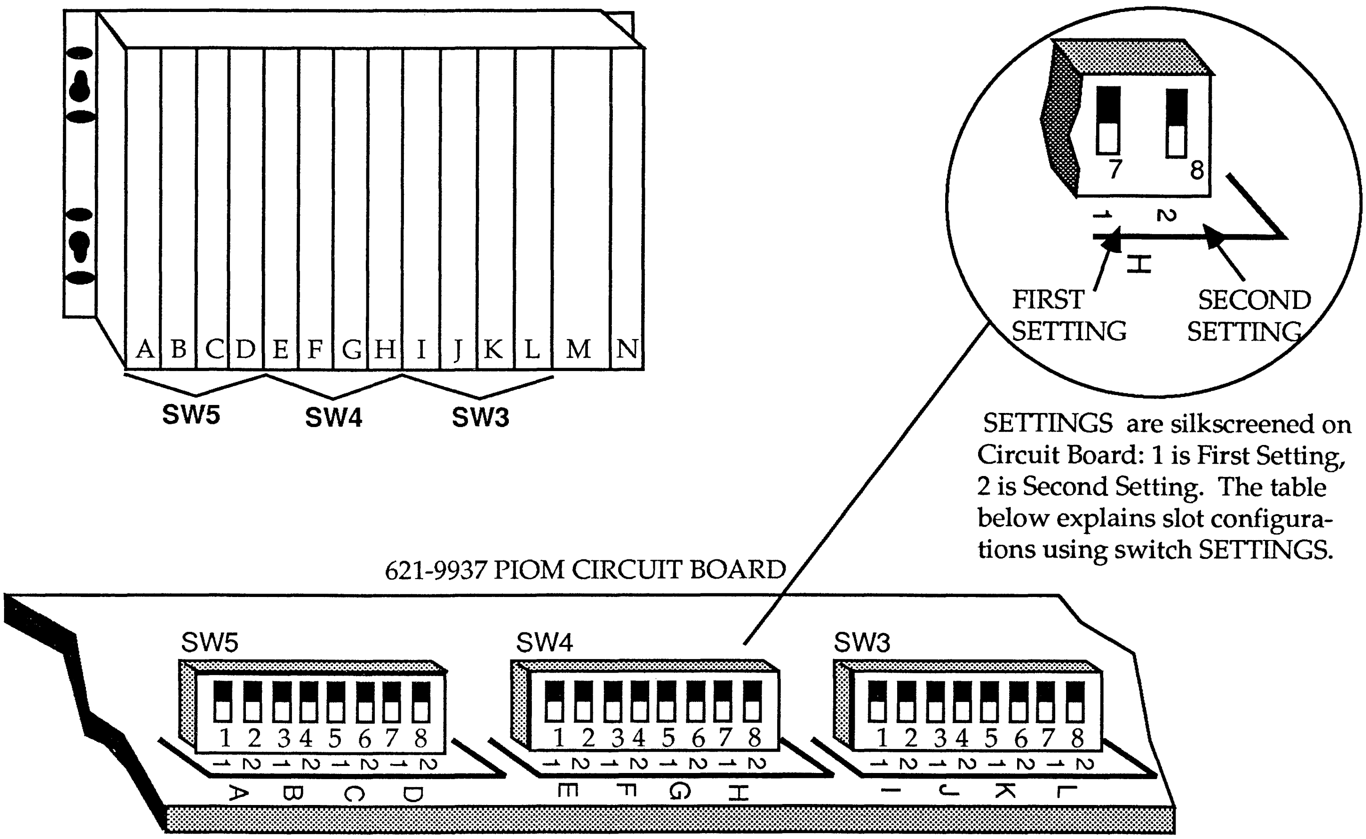
The following procedure describes how to set the point capacity for each I/O slot in the I/O rack. The 621-9937 PIOM DIP switches SW3, SW4, and SW5 are referenced. Refer to Figure 16 while using this procedure.

1. Locate the desired slot by slot letter.

2. Find the DIP switch bank (SW3, SW4, or SW5) that contains the desired slot letter. The corresponding slot letter is silkscreened on the circuit board.

3. Find the pair of DIP switch positions that control the slot's configuration. There are two numbers, a "1" and a "2', silkscreened on the circuit board for each DIP switch pair. Notice that for each DIP switch pair, one switch position is designated as the First Setting (labeled 1) and the other is designated as the Second Setting (labeled 2). For example, slot K is configured by the SW3 DIP switch positions 5 and 6 (position 5 is the First Setting and position 6 is the Second Setting).

4. Refer to Figure 17, SLOT CONFIGURATON SELECTION table. This table lists the settings for 0-, 8-, 16- and 32-point selection. Find the desired point requirements in the table and set the corresponding DIP switch positions.



SLOT CONFIGURATION SELECTION

MODULE TYPE	SETTING FIRST	SETTING SECOND
0-Point	Closed/ON	Closed/ON
8-Point	Open/OFF	Closed/ON
16-Point	Closed/ON	Open/OFF
32-Point*	Open/OFF	Open/OFF

*Factory Setting for all switches

Example:
- Slot C with a 16-point module
  - SW5, position 5 - Closed/ON
  - SW5, position 6 - Open/OFF
- Slot G with an 8-point module
  - SW4, position 5 - Open/OFF
  - SW4, position 6 - Closed/ON

FIGURE 16 - SETTING 621-9937 PIOM DIP SWITCHES

SYSTEM STATUS TABLE

The System Status Table consists of memory locations 8 bits wide. It stores processor system diagnostic information. This information is accessed through the Loader/Terminal by using a four-digit decimal address and a PULL instruction in the control program. The 620-06 processor system instruction set includes the PULL instruction. Three categories of information are stored in the System Status Table: System Diagnostics, System Hardware Status, and System Identification. The more commonly used addresses and register contents are listed in Table 5. Refer to the MS-DOS LOADER 3.0 USER MANUAL (Form 623-8986) for additional System Status Table information and the table access procedures.

TABLE 5 - SYSTEM STATUS TABLE CONTENTS

DECIMAL ADDRESS	REGISTER CONTENTS
2413	Scan loss/battery
2415	Card fault count
2417	Card fault address 8
2419	Card fault address 7
2421	Card fault address 6
2423	Card fault address 5
2425	Card fault address 4
2427	Card fault address 3
2429	Card fault address 2
2431	Card fault address 1
2432	Alternate Model # (In Hex)
2287	Software request for program
2291	Scan time
2295	Force count
2297	Memory used
2299	Memory size
2301	Keyswitch/jumpers
2302	Revision Level (48 is current)

620-06 INSTRUCTION SET

RELAY LOGIC INSTRUCTIONS

Normally Open Contact - Examines an input for an ON condition; examines an output for an energized condition.

Normally Closed Contact - Examines an input for an OFF condition; examines an output for a de-energized condition.

Transition ON Contact - Acts as a one-shot; ON for one scan when its address energizes and OFF thereafter.

Transition OFF Contact - Acts as a one-shot; ON for one scan when its address de-energizes and OFF thereafter.

Branch - Creates parallel branch circuits in a logic line.

Output - Energizes when preceding ladder logic is true.

Retentive Output - Logic status is retained ON or OFF when power is removed. At program power up all retentive outputs assume their last state before the power down.

Latch Output - Energizes when preceding logic is true and remains energized regardless of logic changes. Must be unlatched to be de-energized.

Unlatch Output - De-energizes a latch output with an identical address when preceding logic is true. Remains unlatched regardless of logic changes.

TIMER AND COUNTER INSTRUCTIONS

All timer instructions increment from zero toward the preset value.

ON Delay Timers (0.1 and 1.0 Second) - Begin to time when the preceding logic is true. The output turns ON when the accumulated value equals the preset value. Timer is reset to zero when the preceding logic is false.

OFF Delay Timers (0.1 and 1.0 Second) - Begin to time when preceding logic is false. The output turns OFF when the accumulated value equals preset.

Retentive ON Delay Timer (0.1 and 1.0 Second) - Separate timer RUN and RESET inputs. When the RUN input is false, the timer will not run and the accumulated value is retained. When the RESET input is false, the timer is reset.

Up/Down Counter - Counts from -65,535 to +65,535, transferring an ON signal to the output status table and I/O system when the accumulated value equals the present value.

SKIP INSTRUCTIONS

Not Skip and Retain - When preceding logic is false, all following logic line terminators are skipped, retaining their terminators' present status until a matching End of Skip instruction is encountered.

Not Skip and De-energize - When preceding logic is false, all following logic lines terminators are skipped and their terminators de-energized until an End of Skip instruction is encountered.

End of Skip - Marks the point where memory scan resumes after executing skip or jump instructions.

Return to Beginning of Program - Instructs program scan to return to the beginning of the program.

Jump - When preceding logic is false, all following logic is jumped and not executed until an End of Skip with the specified label is encountered.

Indirect Jump - When preceding logic is false, all following logic is jumped and not executed until an End of Skip with a label specified indirectly by a preceding data instruction is encountered.

SEQUENCER INSTRUCTIONS

Sequencer - Allows processor to store up to 1024 16-bit groups of user-defined data in main memory. The data may be used to control repetitive operations or for bulk data storage.

Load Sequencer - Allows data to be transferred to sequencer tables.

DATA MANIPULATION INSTRUCTIONS

Bring In - Transfers 16 bits of data from the I/O Status Table, or 16 bits plus sign bit from the Register Table, to the processor for use within the logic line.

Send Out - Transfers 16 bits of data from the preceding instructions to the I/O system and the Output status or 16 bits plus sign bit to the Register Table.

PUSH - Transfers multiple 16-bit groups of data from preceding logic to I/O modules (with PUSH/PULL capability), or to the Register Table.

PULL - Transfers multiple 16-bit groups of data from the I/O modules (with PUSH/PULL capability), or the Register Table , to the processor.

Constant - Transfers a number between 0 and 65,535 from the user memory to the processor.

Indirect Bring In - Transfers 16 bits of data from the address pointed to by the Indirect Bring In address in the I/O Status or Register Table. Allows multiplexing of input data.

Indirect Send Out - Transfers 16 bits of data from the preceding data instructions to an address pointed to by the Indirect Send Out address. Allows multiplexing of data.

ARITHMETIC INSTRUCTIONS

Addition - Adds two 16-bit numbers.

Subtraction - Subtracts two 16-bit numbers.

Multiplication - Multiplies two 16-bit numbers.

Division - Divides a 32-bit dividend by a 16-bit divisor to yield a 16-bit quotient and a 16-bit remainder.

Equality Comparison - Compares for equality between two data values.

Less Than Comparison - Compares for less than condition between data values.

Greater Than Comparison - Compares for greater than condition between signed data values.

Test for Zero - Processor tests specified Register or 16 consecutive I/O status table locations for a zero conditon. If a zero condition is detected, the contact will be ON.

MISCELLANEOUS INSTRUCTIONS

Input Status Scan - Temporarily suspends program execution in order to allow the Input Status Table to be updated.

No Operation - A place-holding instruction that facilitates on-line program changes.

TABLE 7 - 620-06 INSTRUCTION SET AND EXECUTION TIMES

INSTRUCTIONS	INSTRUCTION EXECUTION TIMES (Microseconds) MIN.	MAX.	NOTES
RELAY LOGIC			
* NO Contacts	7.92	9.76	A
* NC Contacts	9.76	12.81	A
* Transition ON Contacts	11.59	18.91	
* Transition OFF Contacts	11.59	18.91	
Branch	14.0	–	
* Output	14.03	15.86	A
* Retentive Output	14.03	15.86	A
* Latch Output	14.64	18.27	A, B
* Unlatch Output	15.25	18.91	
TIMER & COUNTER			
0.1 Second ON Delay Timer	35.99	67.71	A
1.0 Second ON Delay Timer	41.48	67.71	A
0.1 Second OFF Delay Timer	30.50	64.05	A
1.0 Second OFF Delay Timer	35.99	62.22	A
0.1 Second Retentive ON Delay Timer	22.57	53.07	
1.0 Second Retentive ON Delay Timer	28.06	53.07	
Up/Down Counter	29.89	50.63	
SKIP			
* Not Skip and Retain	20.13	56.73	
* Not Skip and De-energize	18.60	50.63	
End of Skip	14.64	21.35	
* Return to Beginning of Program	7.30	14.64	
* Jump	20.13	92.11	
* Indirect Jump	28.06	103.70	
SEQUENCER			
Sequencer	49.41	–	
Load Sequencer	38.43	172.02	
MISCELLANEOUS			
Input Status Scan	–	–	C
No Operation	5.49	5.49	
DATA MANIPULATION			
Bring In	23.79	148.84	A
* Send Out	23.79	128.70	A
PUSH	–	–	D
PULL	–	–	D
Constant	27.45	–	
Indirect Bring In	52.46	282.43	A
Indirect Send Out	37.82	283.04	
ARITHMETIC			
Addition	72.59	77.47	
Subtraction	81.13	86.01	
Multiplication	145.18	147.62	
Division	506.30	511.18	
Equality Comparison	55.5	57.94	
Less Than Comparison	55.5	56.73	
Greater Than Comparison	54.29	56.73	
* Test for Zero	–	–	E

* Instructions that may be forced.

NOTES:

A Maximum time to real I/O addresses
B Maximum time when latch is ON
C With no option card -- .42 milliseconds
With a CNM -- 2.32 milliseconds
With any other option card -- .73 milliseconds

D PUSH to real I/O . . . . . .71.37 + N (55.51)
PUSH to register . . . . . . .53.07 + N (21.96)
PULL from real I/O . . . . 40.26 + N (53.07)
PULL from register . . . . .40.26 + N (18.91)
E 16-bit register (4096-4351)......21.96 microseconds
Single-bit register (0-767)......145.79 microseconds

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